Lanmus

LM-40G-QSFP-SR-MM850

DATASHEET

RoHS Compliant 40Gb/s QSFP+ 850nm 100m & 300m Optical Transceiver



PRODUCT INTRODUCTION

Product Overview



LM-40G-QSFP-SR-MM850 is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP+ Transceiver for 40 Gigabit Ethernet Applications. This transceiver is a high-performance module for short-range multi-lane data communication and interconnect applications.

It integrates four data lanes in each direction with 40 Gbps bandwidth. One version is Each lane can operate at 10.5Gbps up to 100m using OM3 or 150m using OM4 Multimode fiber. Another version is each lane can operate at 10.5Gbps up to 300m using OM3 or 400m using OM4 Multimode fiber. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm.

The electrical interface uses a 38-contact edge type connector. The optical interface uses an 12 fiber MTP (MPO) connector. This module incorporates proven circuit and VCSEL technology to provide reliable long life, high performance and consistent service.

PRODUCT INTRODUCTION

Product Features

- Supports 1.06 to 10.5Gb/s bit rates per Channel
- Four-Channel, 1×12 MPO receptacle
- Hot pluggable QSFP+ form factor
- VCSEL 850 nm array Technology
- Applicable for 100m & 300m on OM3 MMF, 150m & 400m on OM4 MMF.
- Built-in digital diagnostic functions
- Low power consumption, <1.5W
- Unretimed XLPPI electrical interface
- Operating case temperature: -5°C to 80°C

Applications

- 40G BASE-SR4 40G Ethernet
- Datacom/Telecom switch & router connections
- Data Aggregation and Backplane Applications
- Proprietary Protocol and Density Applications
- Infiniband transmission at 4CH SDR, DDR and QDR
- Other optical links

Absolute Maximum Ratings

Parameter	Symbol	Max.	Min.	Unit	Note
Supply Voltage	Vcc	-0.5	3.6	V	
Storage Temperature	TS	-20	85	°C	
Relative Humidity	RH	0	85	%	
Damage Threshold, per Lane	DT	3.4		dBm	

Note: Stress in excess of the maximum absolute ratings can cause permanent damage to the transceiver.

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General Operating Characteristics

Parameter	Value	Unit	Note
Module Form Factor	QSFP+		
Number of Lanes	4Tx and 4Rx		
Maximum Aggregate Data Rate	42.0	Gb/s	
Maximum Data Rate per Lane	10.5	Gb/s	
Protocols Supported	Typical applications include 40G Ethernet, InfiniBand, Fibre Channel, SATA/SAS3		
Electrical Interface and Pin-out	38-pin edge connector, Pin-out as defined by the QSFP+MSA		
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		

Parameter	Symbol	Min	Type	Max	Units	Note
Bit Rate per Lane	B_R	1062		10500	Mb/sec	1
Bit Error Ratio	B_{ER}			10-12		2
Distance on OM3 MMF (CDS1)	D_1			100	meters	3
Distance on OM4 MMF (CDS1)	D_2			150	meters	3
Distance on OM3 MMF (CDS3)	D_3			300	meters	4

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Parameter	Symbol	Min	Type	Max	Units	Note
Distance on OM4 MMF (CDS3)	D_4			400	meters	4

Notes:

1. Compliant with 40G Ethernet. Compatible with 1/10 Gigabit Ethernet and 1/2/4/8/10G Fibre Channel.
2. Tested with a PRBS 231-1 test pattern.
3. Per 40GBASE-SR4, IEEE 802.3ba, Belong to part No: OLSQ854XM-CDS1
4. Per 40GBASE-SR4, IEEE 802.3ba, Belong to part No: OLSQ854XM-CDS3

Optical Characteristics

(TOP(C) = 0 to 70 , TOP(I) =–40 to 80 , VCC = 3.13 to 3.47 V)

Parameter	Symbol	Min	Type	Max	Units	Note
Transmitter						
Operating Wavelength	λ	840	850	860	nm	
Ave. output power (Enabled)	P_{AVE}	-7.5		+2.5	DbM	
Difference in launch power between any two lanes (OMA)	D_L			4	dB	
Extinction Ratio	E_R	3			dB	
Peak power, each lane	P_P			4	dBm	
Dispersion penalty, each lane	T_{DP}			3.5	dB	
Average launch power of OFF transmitter, each lane	P_{OFF}			-30	dB	
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4					Hit Ratio= 5×10-5

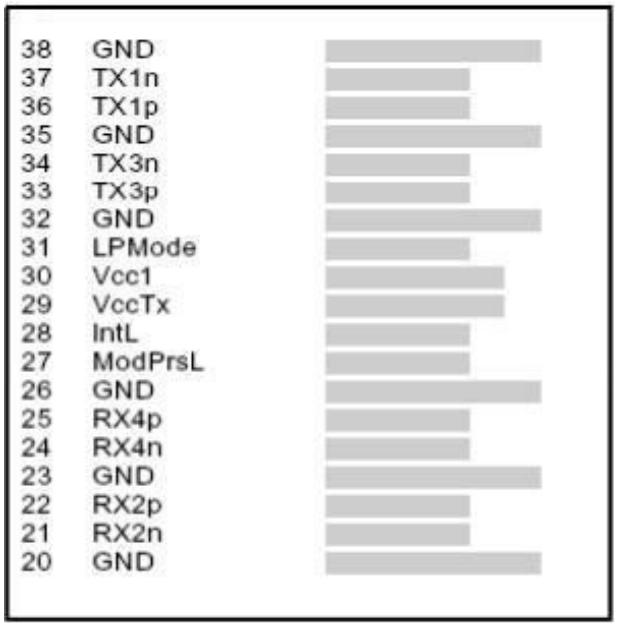
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Receiver						
Operating Wavelength	λc	840	850	860	nm	
Stressed receiver sensitivity in OMA (OLSQ854XM-CDS1)	P_{SEN1}			-5.4	dBm	3
Stressed receiver sensitivity in OMA (OLSQ854XM-CDS3)	P_{SEN2}			-7.5	dBm	3
Average Receive Power, each lane	P_{AVE}	-11		+2.4	dBm	
Receiver Reflectance	R_{rx}			-12	dB	
LOS Assert	P_a	-30			dBm	
LOS De-assert	P_d			-9	dBm	
LOS Hysteresis	P_d-P_a	0.5			dB	

Notes:

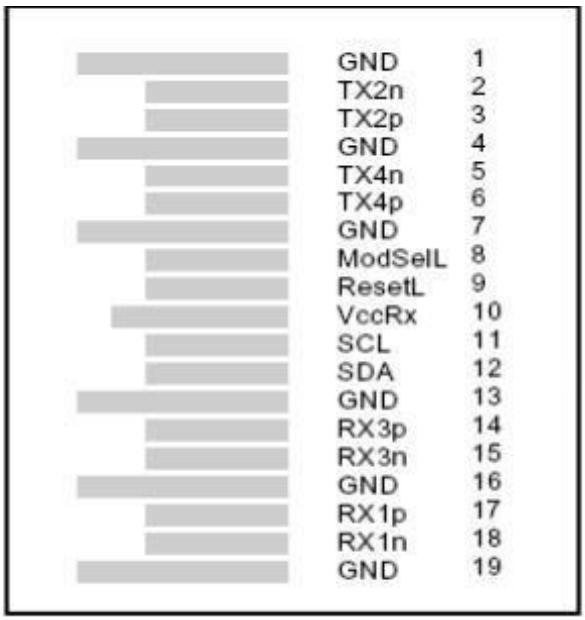
1. Measured with conformance test signal at TP3 for BER=10-12 Receiver Characteristics

Pin Definition and Functions



TOP SIDE

LM-40G-QSFP-SR-MM850



BOTTOM SIDE

Pin Definition and Functions

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	1
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power supply receiver	

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Pin	Symbol	Name/Description	Notes
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver	Non-Inverted
23	Rx2p	Receiver Non-Inverted Data Output	
24	GND	Ground	1
25	Rx4n	Receiver Inverted Data Output	
26	Rx4p	Receiver Non-Inverted Data Output	
27	GND	Ground	1
28	ModPrsL	Module Present	
29	IntL	Interrupt	

Pin	Symbol	Name/Description	Notes
30	Vcc Tx	+3.3V Power supply transmitter	
31	Vcc1	+3.3V Power Supply	
32	LPMode	Low Power Mode	
33	GND	Ground	1
34	Tx3p	Transmitter Non-Inverted Data Input	
35	Tx3n	Transmitter Inverted Data Input	
36	GND	Ground	1
37	Tx1p	Transmitter Non-Inverted Data Input	
38	Tx1n	Transmitter Inverted Data Input	
39	GND	Ground	1

Notes

1. Circuit ground is internally isolated from chassis ground.

Other Pin Description:

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

ResetLP Mode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.

During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Rayoptek PSM IR4operate in the low power mode (less than 1.5W power consumption) This pin active high will decrease power consumption to less than 1W.

Notes

ModPrsL Pin

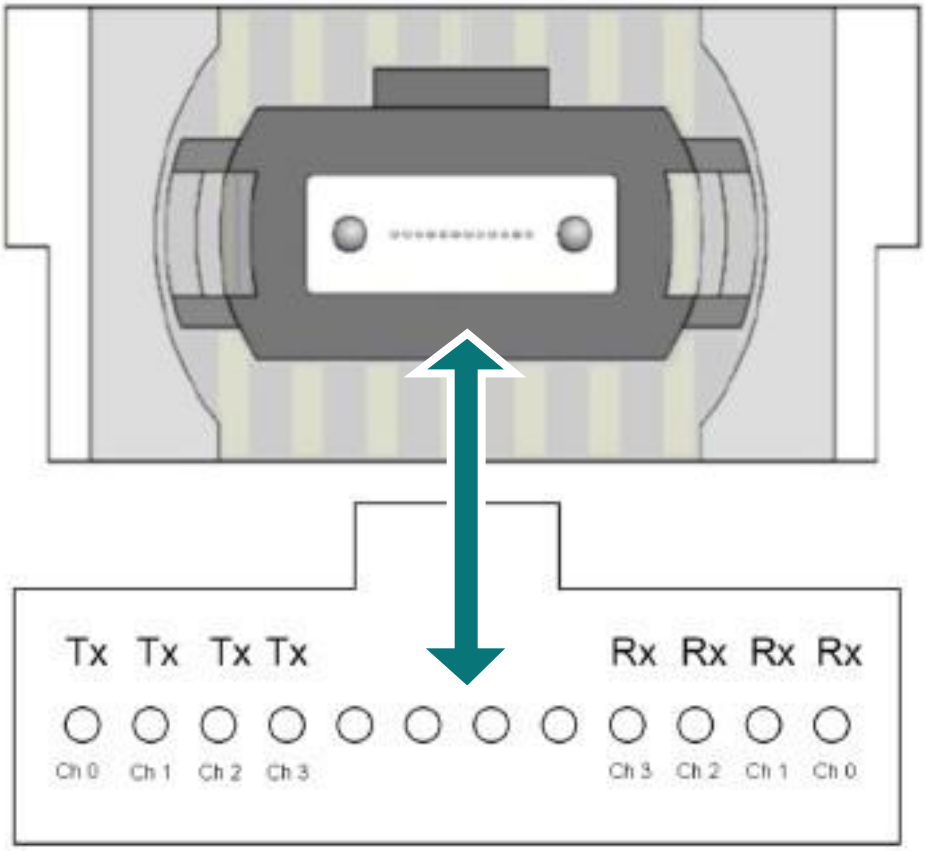
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and de-asserted “High” when the module is physically absent from the host connector.

IntL Pin

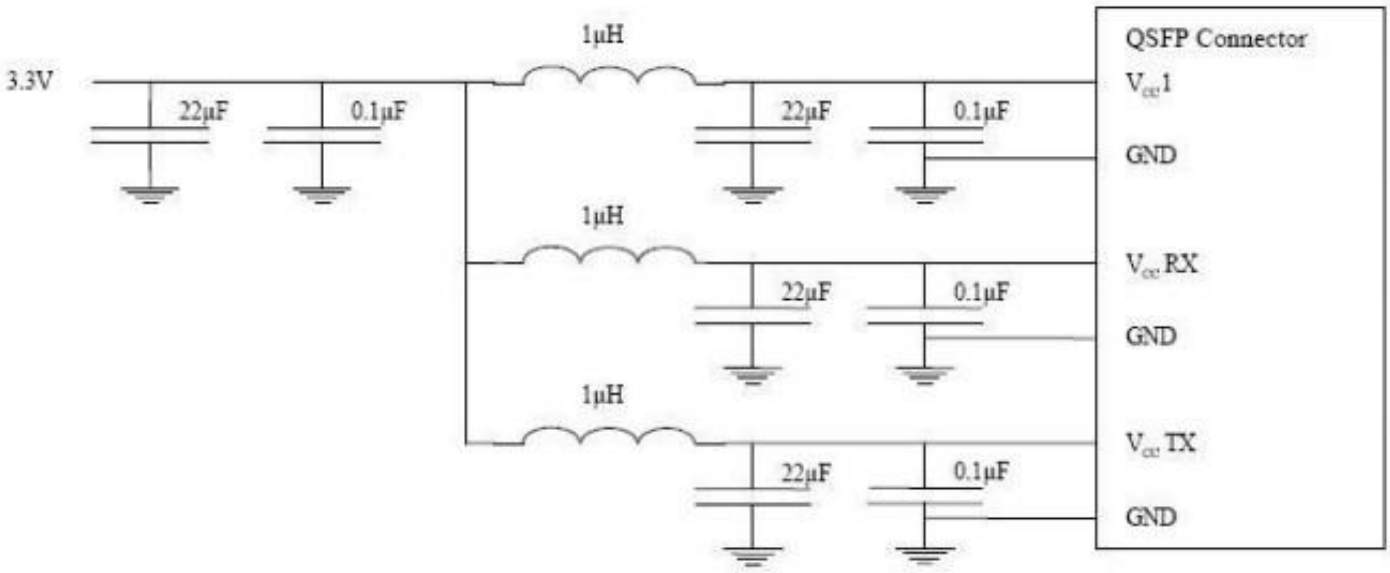
IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Optical lane assignment

Front view of MPO receptacle

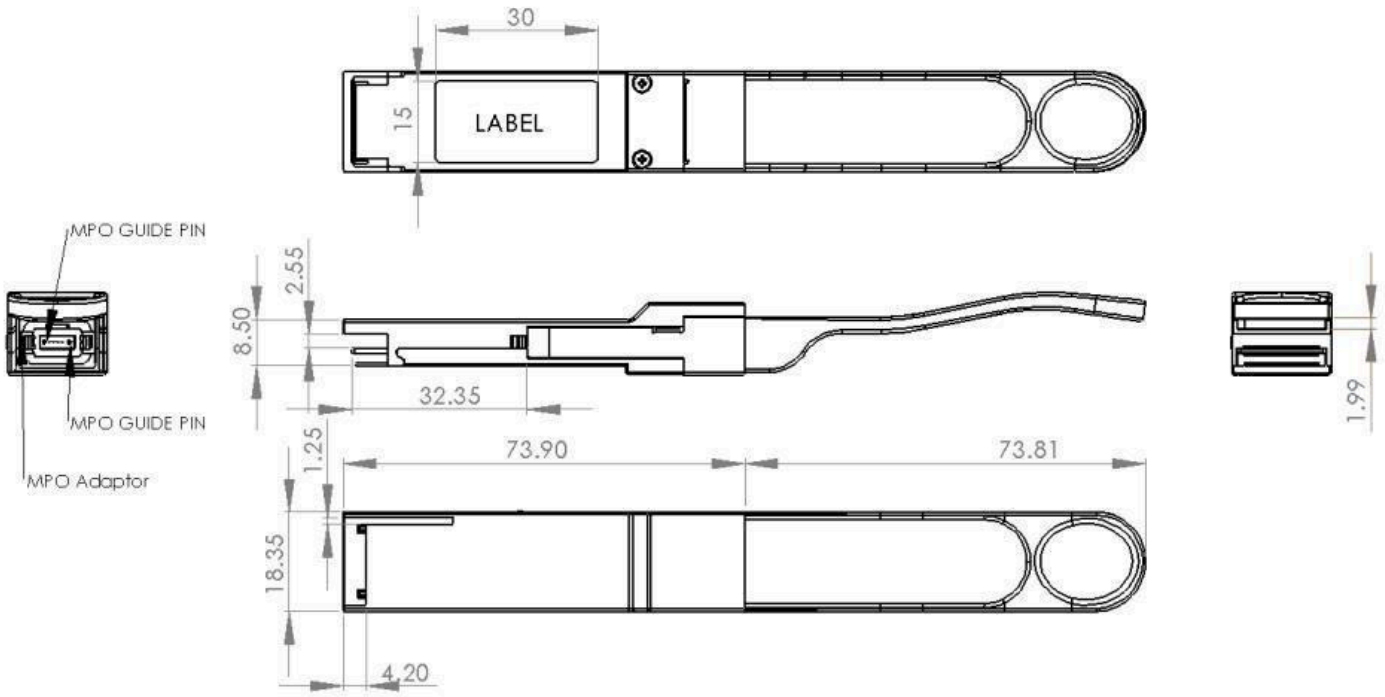


Power Supply Filtering



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Package Dimensions



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Lanmus Accessories

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